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EFFICIENT SINGLE PHASE TO THREE PHASE CONVERTER USING SPACE VECTOR MODULE

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Abstract- Sinusoidal PWM has been an extremely well known strategy utilized in AC engine control. This generally unsophisticated strategy utilizes a three-sided transporter wave balanced by a sine wave and the places of convergence decide the exchanging points of the force gadgets in the inverter. Be that as it may, this strategy can't utilize the inverter's stockpile voltage and the uneven idea of the PWM exchanging qualities creates moderately high consonant mutilation in the inventory.

Space Vector PWM (SVPWM) is a more refined strategy for producing a crucial sine wave that gives a higher voltage to the engine and lower all out symphonious twisting (THD). It is additionally viable for use in vector control (Field direction) of AC engines. This theoretical depicts the hypothesis of SVPWM and the undertaking will be made utilizing a modified microcontroller of 8051 family appropriately interfaced to 3 stage six heartbeat inverter with 6 no's MOSFET from DC gotten from a solitary stage mains or 3 stage, 50 Hz supply. The heap will be a three stage 50 Hz 440volt 0.5 HP engine. Then again a star light burden can be utilized instead of engine to see the waveform as it were.

Further this venture can be upgraded by utilizing IGBT rather than MOSFET for higher voltage power tasks. Speed control of the engine can likewise be accomplished by V/F strategy.

Index Terms- Space Vector Modulation, Single phase to three phase converter, Capacitor volume reduction

I. INTRODUCTION

Staggered inverters produce sinusoidal voltages from discrete voltage levels, and pulse width modulation (PWM) procedures achieve this errand of creating sinusoids of variable voltage and recurrence.

frequency. Modulation methods fo Hybrid Multilevel Inverter can be classified according to Switching frequency methods. Various PWM techniques have been created to accomplish the accompanying: Wide straight adjustment range, less exchanging misfortune, diminished Total Harmonic Distortion (THD) in the range of exchanging waveform.: and easy implementing the pulse width Modulation (PWM) strategy for multilevel inverters are Sinusoidal PWM (SVPWM). The SPVWM is considered as a better technique of PWM implementation as it has advantages over SVPWM in terms of dc bus voltage, reduced switching frequency and low current ripple is presented in Beig et al (2007), Guptaand Khambadkone (2007), and Franquelo et al (2006).

II. METHODOLOGY

Single Phase input ac supply of 230V, 50Hz is stepped down using transformer. This voltage is then converted into dc using bridge and filter. The filtered output is provided to microcontroller by regulating it to 5V as microcontroller need 5V for its working. In the same way the gate driver also works on 16V, so the same filtered output is regulated to 16V and provided to the gate driver.

For three phase conversion, 230V ac to 230V dc conversion is required. This conversion is done using bridge rectifier and capacitor bank. For three phase conversion power module is used which includes bank of IGBT in H-bridge configuration. To convert single phase to three phase, space vector pulse width modulation techniques are used. Space vector PWM is generated using microcontroller and is provided to the power module using gate driver. Gate driver is used to drive MOSFET in threshold zone with maintaining sync current.

III. BLOCK DIAGRAM

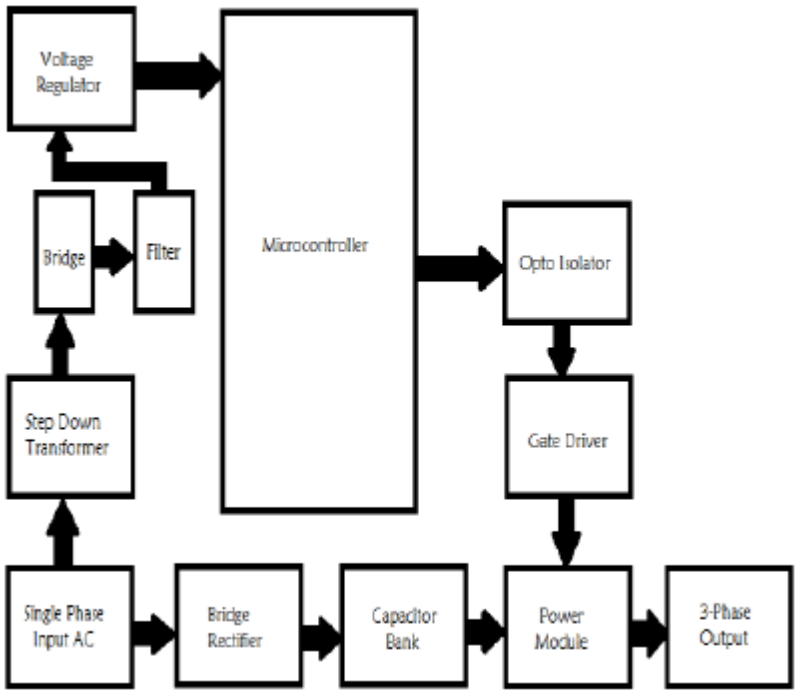

Fig.1 Block Diagram Explanation

This task essentially involves a 3-ph inverter where key sine wave is contrasted with create heartbeat width regulated signals so produced by a program composed onto the microcontroller. This yield is taken care of to a bunch of six opto-isolators, U1 to U6 (MCT2E) from one of the ports of the MC i.e., PORT-0 from pin no. 34 to 39. The objective of using opto-isolator is to achieve galvanic isolation between the low voltage control circuit to the high voltage power circuits comprising of six no's of power changes like MOSFETs Q1 to Q6 (IRF730), 3 for the top bank and equilibrium 3 for the base bank. Snubber circuits comprising of resistors (R21-R26), diodes (D25-D30) and capacitors (C11-C16) are provided across the drain, source of each of the MOSFET to take care of the inductive loads. The base bank wellspring of MOSFET has ground reference. Therefore driving them through control signal is easy. Anyway driving the main three it is troublesome as they have no ground reference. In order to overcome such problem 3 no's of driver ICs U7, U8, U9 (IR2101) are used, each driver handling a pair of power switches in complementary mode to make sure that both of the power switches do not conduct simultaneously (for e.g. Q1 and Q4) which would otherwise cause a short circuit of the DC power fed to the bank. Boot strap capacitors C5, C7 & C9 in combination with D1, D2 & D3 of the circuit, SVPWM 2 of 3 take care of the control supply source of the 3 top power switches. The high voltage DC power is derived directly from 230V AC source after rectification by a power bridge rectifier duly filtered by capacitors and this dc is fed through a series lamp for precaution purposes to the 3 phase MOSFET bridge.

The control power necessity is accomplished by little low force transformers, connect rectifier and the channel capacitor in the degree of 12V to 15V territory. MC power prerequisite of 5V is gotten from the 12V source.Three phase output is taken from the junction points of top MOSFETs source and the bottom MOSFET's drain.

IV. VOLTAGE SPACE VECTORS

Space Vector Modulation (SVM) for three-leg VSI relies upon there presentation of the three phase amounts as vectors in a two-dimensional(,) plane. Considering geography 1 of Figure 4.2, which is rehashed in Figure 4.3 a. The line voltages *Vab* ,*Vb c* and *Vca* are given by

$$Vab = +Vdc$$
$$Vbc = 0$$
$$Vca = -Vdc$$

This can be represented in the (,) plane as shown in Figure4.3(b), where voltages *Vab* ,*Vbc* and *Vca* are three line voltage vectors displaced 1200 in space. The effective voltage vector generated by this topology is represented as *V*1 (pnn) in Figure 4.3.b .The exchanging network appeared in Figure 4.1 has an aggregate of eight potential exchanging mixes. Each exchanging mix is appeared in Figure 4.2, and is addressed by the stage leg association, where 'p' indicates that stage leg is associated with the positive rail of the DC connection, and 'n' means that stage leg is associated with the negative rail of the DC interface. For instance, exchanging mix 'pnn' addresses the condition where the phase A output terminal *Va* is connected to the positive DC rail, and phase B and C.

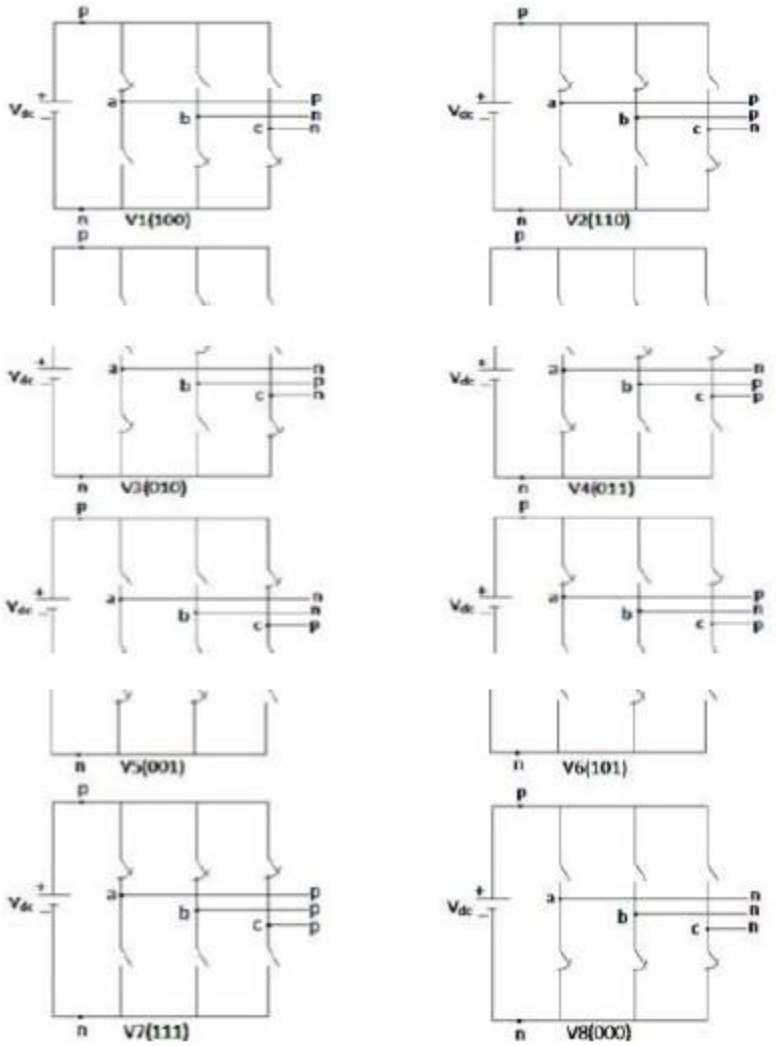

Figure 4.2 Eight Switching Stage Topographies of Three-Phase Inverter

Each exchanging blend brings about a bunch of three stage voltages at the AC terminal of the exchanging organization. A reference vector *V*1 can be obtained by transforming the reference three-phase voltage into the α - β. A balanced three-phase sinusoidal waveformis obtained when the reference vector is rotating in the α – β plane.
Continuing on comparative lines the six non-zero voltage vectors can be appeared to expect the positions appeared in Figure 4.4. The tips of these vectors structure a standard hexagon (spotted line appeared in Figure 4.4).The region encased by two adjoining vectors, inside the hexagon, is picked as an area. In this manner there are six areas numbered 1 to 6 in Figure 4.4.

V. CIRCUIT TOPOLOGY

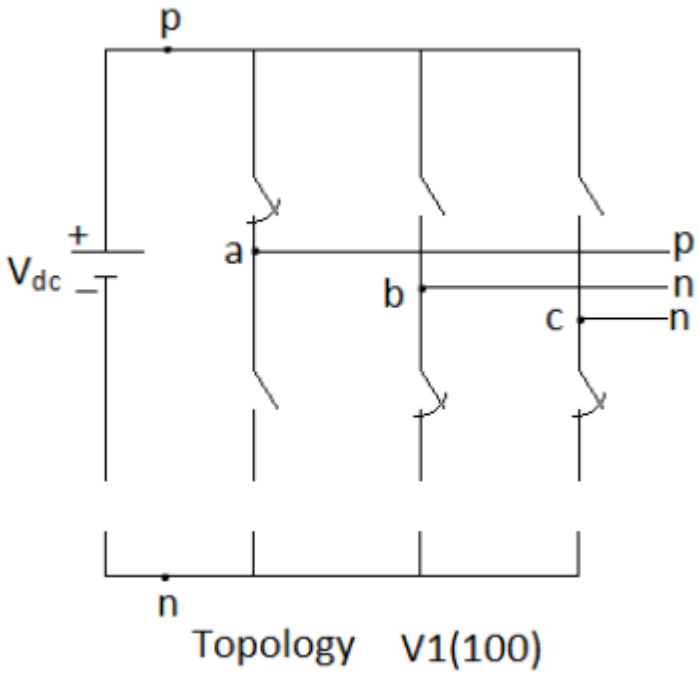

Figure 4.3.a. Topology V1 (100) Voltage Source Inverter

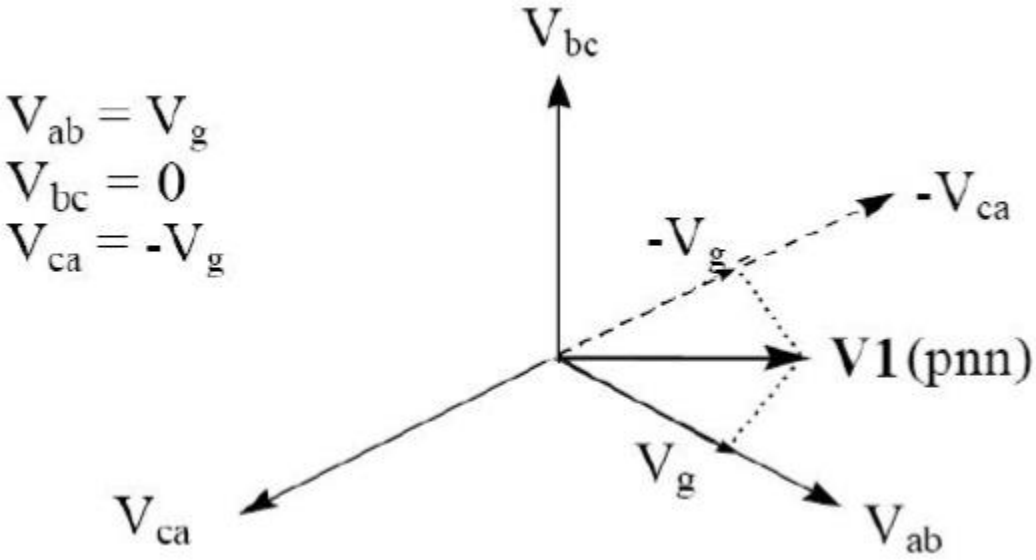

Figure 4.3.b. Topology Representation of α , β plane

The yield line voltages produced by this topology in Figure 4.5.a are given by

Vab = 0
Vcb = 0
Vca = 0

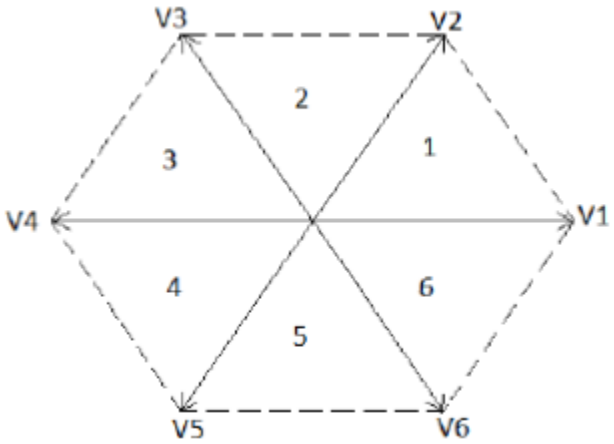

Figure 4.4 Non-Zero Voltage Vectors in the α, β plane.

The yield voltages are addressed as vectors which have zero greatness and henceforth are alluded to as zero-exchanging state vectors or zero voltage vectors. The situation at starting point in the (,)plane is demonstrated in Figure 4.5.b. A sum of eight vectors are acquired by changing the three-stage voltages into the a b organize and the equivalent are called exchanging state vectors.

VI. SPACE VECTOR MODULATION

The ideal three stage voltages at the yield of the inverter could be addressed by a comparable vector V pivoting in the counter clock shrewd heading as demonstrated in Figure 4.6.a. . The greatness of this vector is identified with the extent of the yield voltage as demonstrated in Figure 4.6.b and the time this vector takes to finish one upset is equivalent to the crucial time-frame of the yield voltage.

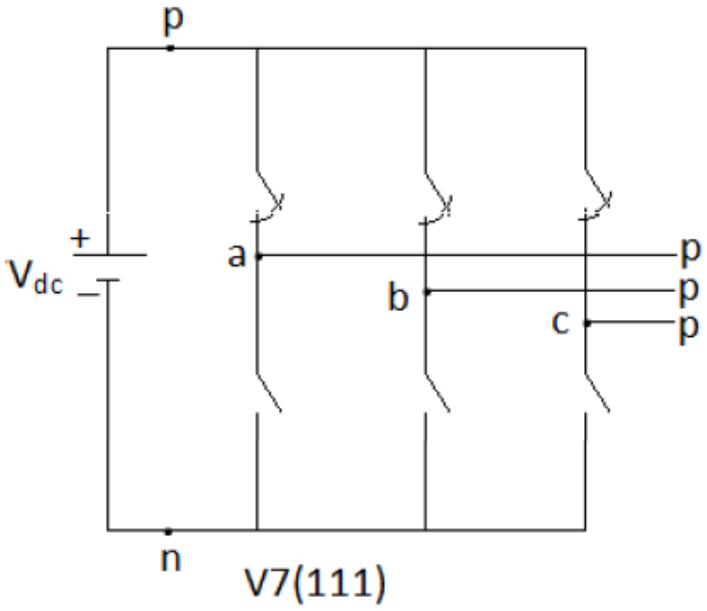

Figure 4.5.a. Zero Output Voltage Topologies

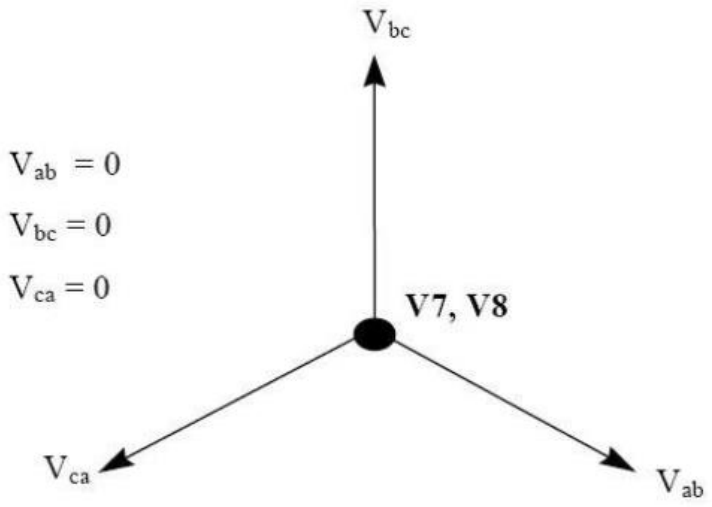

Figure 4.5.b Representation of the zero voltage vectors in the α , β plane.

At the point when the ideal line-to-line yield voltage vector V is in area 1 as demonstrated in Figure 4.7., vector V could be blended by the beat width balance (PWM) of the two nearby exchanging state vectors V1 (pnn) and V2 (ppn), the obligation pattern of each being d1 and d2, individually, and the zero vector (V7 (nnn)/V8 (ppp)) of obligation cycle d0:

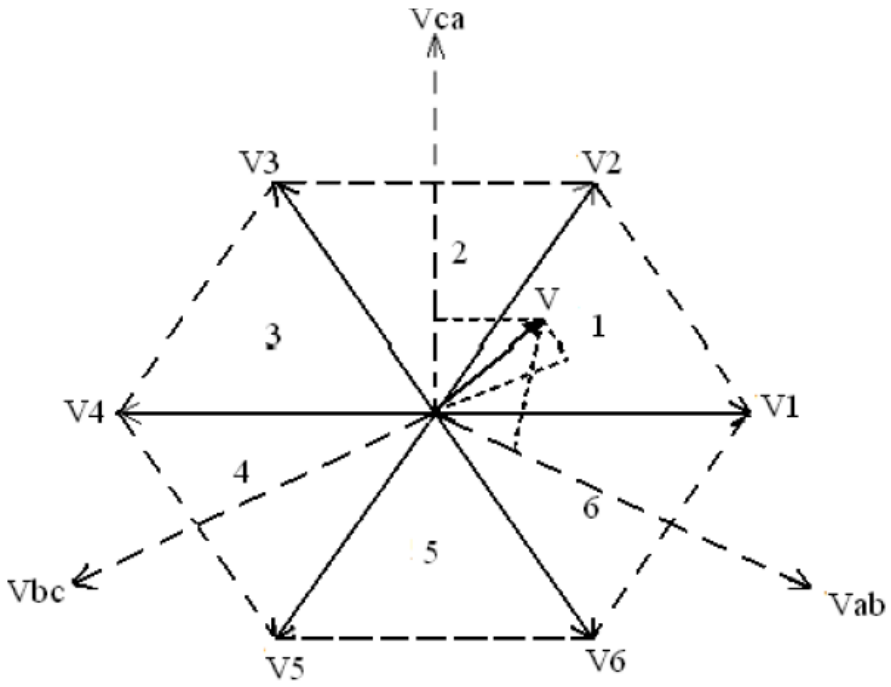

Figure 4.6.a Output voltage vector in the α , β plane.

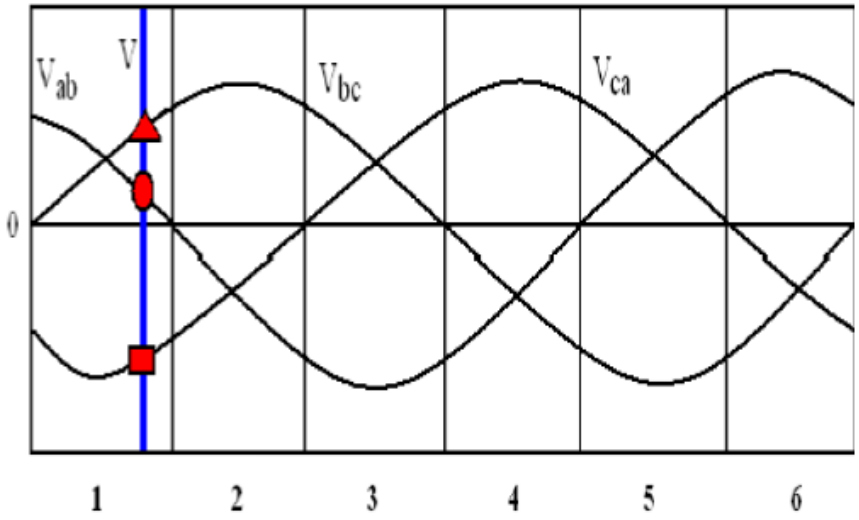

Figure 4.6.b Output Line Voltage

VII. GENERAL STRUCTURE OF THE ALGORITHM

The control processing unit calculates the basic parameters to apply a switching state. The input information to the control handling unit is the reference space vector. During various iterations, the unit determines the sector number, triangle number of the sub hexagon. The area number and triangle number recognize the right exchanging grouping The flowchart is given for a n-level inverter and can be utilized for any n-levels without change.. The input supply is the abundancy of the voltage steps and tweak file m, the underlying estimation of o The stream chart of the proposed calculation to discover least THD is appeared in Figure 4.8 .. The balance list mc is determined for different cycles. The contrast between two adjustment file terms is determined.

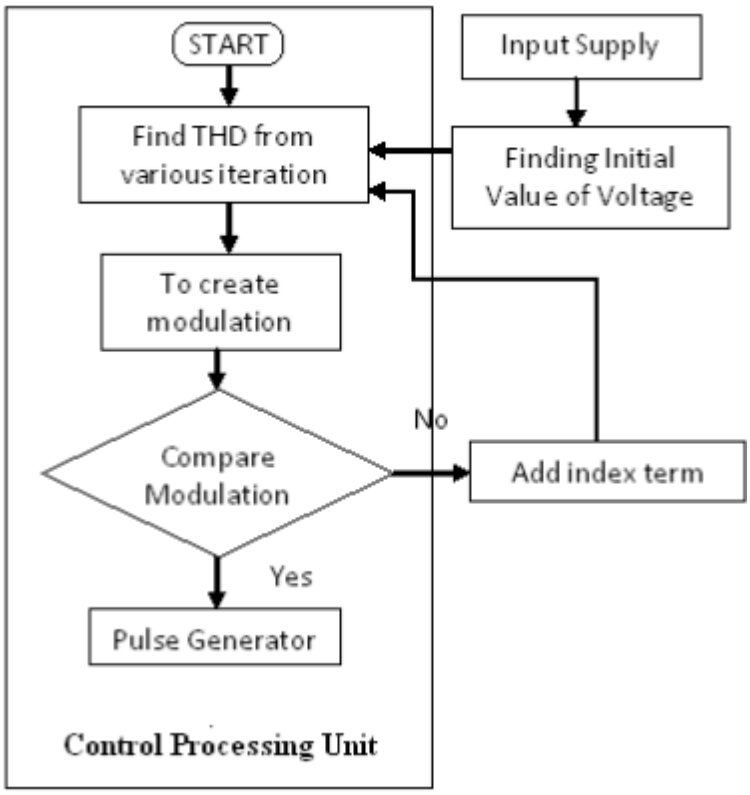

Figure 4.8 Flowchart of the Algorithm

$|m - mc| = \delta$ (4.20)

Where,

δ is the Reference value increases (or) decreases the pulse generation in the pulse generator. If the difference between the two modulation index terms is less than reference value , the proposed algorithm outputs the optimal switching angles. The emphasis strategy is utilized to settle and discover minimization of the voltage THD.

VIII. COMPARISON OF SVPWM AND PWM

The SVPWM is considered a better technique of PWM implementation as it has some advantages over SPWM in terms of good utilization of dc-bus voltage, reduced switching frequency and low current ripple. . SVPWM gives the accompanying benefits: I) better crucial yield voltage; ii) helpful in improving consonant execution and diminishing THD; and iii) simpler equipment execution in advanced sign processor. SVPWM can be productively executed in a couple of miniature seconds, accomplishing comparative outcomes contrasted and other PWM strategies

IX. CONCLUSION

In this section, two effective SVPWM strategies were talked about . The basic idea about SVPWM for three-legged voltage source inverter was discussed in detail. It is illustrated how the voltage space vectors are defined in a two-dimensional (2-D) plane and three-dimensional (3-D) plane for a cascaded H-bridge multilevel

inverter. Moreover, two dimensional (2-D) and three-dimensional (3-D) space vector regulation calculations are clarified. Numerical definition for figuring exchanging points and exchanging grouping was resolved and the Fourier arrangement hypothesis was utilized to infer the symphonious conditions relating to the staggered exchanging plan.

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